

IN THE CLAIMS

1 **Claim 1 (currently amended): A method for fabricating a silicon based package (SBP) in**
2 **the sequence as follows:**

3 **starting with a wafer composed of silicon and having a first surface and a reverse**
4 **surface which are planar as the base for the SBP,**

5 **then forming an interconnection structure including multilayer conductor patterns**
6 **over the first surface; [,]]**

7 **then forming a protective overcoat layer over the interconnection structure; [, and]]**

8 **then forming a temporary bond between the protective overcoat layer of the SBP and**
9 **a wafer holder, with the wafer holder being a rigid structure; [,]]**

10 **then thinning the reverse surface of the wafer to a desired thickness to form an ultra**
11 **thin silicon wafer (UTSW) for the SBP; [,]]**

12 **then forming via holes which extend through the UTSW; [,]]**

13 **then forming metallization in the via holes with the metallization extending through**
14 **the UTSW; and**

15 **then remove removing the temporary bond.**

1 **Claim 2 (previously presented): The method of claim 1 including bonding the metallization**
2 **in the via holes to pads of a carrier.**

1 **Claim 3 (previously presented): The method of claim 1 including forming capture pads on**
2 **the first surface prior to thinning the wafer.**

1 **Claim 4 (currently amended): The method of claim 1 including:**

2 **initially forming capture pads on the first surface; [,]]**

3 **then forming the interconnection structure over the first surface and the capture**
4 **pads; [,]]**

5 **then forming the temporary bond of the wafer holder to the reverse surface; [,]] and**
6 **then thinning the wafer, thereby forming the UTSW.**

1 **Claim 5 (currently amended): The method of claim 1 including:**
2 **initially forming capture pads on the first surface; [,]**
3 **then forming interconnection structure over the first surface and the capture pads;**
4 **[,]**
5 **then forming the temporary bond of the wafer holder to the reverse surface,**
6 **then thinning the wafer, thereby forming the UTSW; [,] and**
7 **then forming the via holes through the UTSW down to the capture pads.**

1 **Claim 6 (currently amended): The method of claim 1 including:**
2 **initially forming capture pads on the first surface; [,]**
3 **then forming interconnection structure over the first surface and the capture pads,**
4 **then forming the temporary bond of the wafer holder to the reverse surface,**
5 **then thinning the wafer, thereby forming the UTSW; [,]**
6 **then forming the via holes through the UTSW down to the capture pads; [,]**
7 **then forming a dielectric layer over the surface of the wafer leaving the bottoms of the**
8 **via holes clear with the capture pads exposed; [,] and**
9 **then forming the metallization in the via holes in contact with the capture pads.**

1 **Claim 7 (currently amended): The method of claim 1 including:**
2 **initially forming capture pads on the first surface; [,]**
3 **then forming interconnection structure over the first surface and the capture pads**
4 **then forming the temporary bond of the wafer holder to the reverse surface; [,]**
5 **then thinning the wafer, thereby forming the UTSW; [,]**
6 **then forming the via holes through the UTSW down to the capture pads; [,]**
7 **then forming a dielectric layer over the surface of the wafer leaving the bottoms of the**
8 **via holes clear with the capture pads exposed; [,]**
9 **then depositing metal pads into the via holes in contact with the capture pads; [,]**
10 **and**
11 **then [[form]] forming metal joining structures on the metal pads.**

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1 **Claim 8 (previously presented): The method of claim 1 including initially forming via holes**
2 **in the first surface prior to thinning the wafer.**

1 **Claim 9 (currently amended): The method of claim 1 including the steps as follows:**
2 **initially forming via holes in the first surface prior to thinning the wafer; [,]**
3 **then forming a dielectric layer covering the via holes.**

1 **Claim 10 (currently amended): The method of claim 1 including the steps as follows:**
2 **initially forming via holes in the first surface prior to thinning the wafer; [,]**
3 **then forming a dielectric layer over the surface of the wafer including the via holes;**
4 **[,] and**
5 **then forming a through via/cap pad layer of a first metal layer over dielectric layer**
6 **including the via holes.**

1 **Claim 11 (currently amended): The method of claim 1 including the steps as follows:**
2 **initially forming via holes in the first surface prior to thinning the wafer; [,]**
3 **then forming a dielectric layer over the surface of the wafer including the via holes,**
4 **then forming a through via/cap pad layer of a first metal layer over dielectric layer**
5 **including the via holes; [,] and**
6 **then planarizing to remove the via/cap pad layer above the surface of the dielectric**
7 **layer, thereby forming vias in the via holes.**

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1 **Claim 12 (currently amended): The method of claim 1 including the steps as follows:**
2 initially forming via holes in the first surface prior to thinning the wafer; [[,]]
3 then forming a dielectric layer over the surface of the wafer including the via holes,
4 then forming a through via/cap pad layer of a first metal layer over dielectric layer
5 including the via holes; [,,]
6 then planarizing to remove the via/cap pad layer above the surface of the dielectric
7 layer, thereby forming vias in the via holes; [,,] and
8 then forming an interconnection structure over the first surface including the first
9 metal layer.

1 **Claim 13 (currently amended): The method of claim 1 including the steps as follows:**
2 initially forming via holes in the first surface prior to thinning the wafer; [,,]
3 then forming a dielectric layer over the surface of the wafer including the via holes,
4 then forming a through via/cap pad layer of a first metal layer over dielectric layer
5 including the via holes; [,,]
6 then planarizing to remove the via/cap pad layer above the surface of the dielectric
7 layer, thereby forming vias in the via holes ; [,,[and]]
8 then forming interconnection structure over the first surface including the metal vias
9 and the first metal layer; [,,]
10 then forming the temporary bond to the rigid wafer holder on the reverse surface;
11 [,,] and
12 then thinning the wafer to the desired thickness of the UTSW.

**Please cancel claims 14-16 without prejudice to pursuit of the subject matter thereof
in a divisional application.**

Claims 14 - 24 (canceled)

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1 **Claim 25 (currently amended): A method for fabricating a Silicon Based Package (SBP) in
2 the sequence as follows:**

3 **starting with a wafer composed of silicon and having a first surface and a reverse
4 surface which are planar as the base for the SBP; [,]]**

5 **then forming an interconnection structure including multilayer conductor patterns
6 over the first surface; [,]]**

7 **then forming a protective overcoat layer composed of polyimide over the
8 interconnection structure; [,]]**

9 **then forming a temporary bond between the protective overcoat layer of the SBP and
10 a wafer holder, with the wafer holder being a rigid structure; [,]]**

11 **then thinning the reverse surface of the wafer to a desired thickness to form an Ultra
12 Thin Silicon Wafer (UTSW) for the SBP; [,]]**

13 **then forming via holes which extend through the UTSW; [,]]**

14 **then forming metallization in the via holes with the metallization extending through
15 the UTSW; [,]] and**

16 **then removing the temporary bond.**

1 **Claim 26 (currently amended): The method of claim 25 including:**

2 **forming the temporary bond with polyimide; [,]], and**

3 **releasing the temporary bond by laser ablation.**

**Please cancel claim 27 without prejudice to pursuit of the subject matter thereof in a
divisional application.**

Claims 27 (canceled)

1 **Claim 30 (currently amended): The method of claim 1 [[29]] including the UTSW having a
2 desired thickness including the steps performed in the sequence as follows:**

3 ~~performing a step of forming an interconnection structure including multilayer~~
4 ~~conductor patterns over the first surface of the silicon wafer;~~

5 ~~then forming a protective overcoat layer over the interconnection structure;~~

6 ~~[[then]] the step of forming the temporary bond between the protective overcoat layer~~
7 ~~of the SBP and the wafer holder leaving the reverse surface exposed;~~

8 ~~then thinning the reverse surface of the wafer to a desired thickness to form the~~
9 ~~UTSW for the SBP;~~

10 ~~then forming the via holes which extend extending through the thickness of the~~
11 ~~UTSW; and~~

12 ~~then forming the metallization in the via holes with the metallization extending~~
13 ~~through the thickness of the UTSW, [[; and]]~~

14 ~~thereafter releasing the temporary bond.~~

 Please cancel claim 31 without prejudice to pursuit of the subject matter thereof in a
divisional application.

Claim 31 (canceled)